METHOD AND APPARATUS FOR MULTITHREADING ON A PROGRAMMABLE LOGIC DEVICE

ABSTRACT

Programmable architecture for implementing a message processing system using an integrated circuit is described. In an example, configurable logic of the integrated circuit is configured to have a plurality of thread circuits and an interconnection topology amongst the plurality of thread circuits. Messages are concurrently processed using the plurality of thread circuits. Operation of at least one thread circuit of the plurality of thread circuits is controlled in accordance with control data received via the interconnection topology from at least one other thread circuit of the plurality of thread circuits.